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(71) Applicant:
Agilent Technologies Inc.
Santa Clara, California 95052-8043 (US)

(72) Inventors:
- **Cao, Min**
Mountain View, CA 94040 (US)
- **Theil, Jeremy A.**
Mountain View, CA 94040 (US)
- **Ray, Gary W.**
Mountain View, CA 94043 (US)
- **Vook, Dietrich W.**
Menlo PArk, CA 94025 (US)

(74) Representative:
Tollett, Ian et al
Williams, Powell & Associates,
4 St. Paul's Churchyard Inn
London EC4M 8AY (GB)

(54) **Image sensor array device**

(57) An image sensor array. The image sensor array includes a substrate [200]. An interconnect structure [210] is formed adjacent to the substrate [200]. An amorphous silicon electrode layer [250] is adjacent to the interconnect structure [210]. The amorphous silicon electrode layer [250] includes electrode ion implantation regions [240]] between pixel electrode regions [230]. The pixel electrode regions [230] define cathodes of an array of image sensors. The electrode ion implantation regions [240] provide physical isolation between the pixel electrode regions [230]. The cathodes are electrically connected to the interconnect structure [210]. An amorphous silicon I-layer [260] is adjacent to the amorphous silicon electrode layer [250]. The amorphous silicon I-layer [260] forms an inner layer of each of the image sensors. A transparent electrode layer [280] is formed adjacent to the image sensors. An inner surface of the transparent electrode layer [280] is electrically connected to anodes of the image sensors and the interconnect structure [210]. The amorphous silicon I-layer [260] can further include I-layer ion implantation regions [320] that provide physical isolation between the inner layers of the image sensors. The I-layer ion implantation regions [320] align with the electrode ion implantation regions [320]. An amorphous silicon P-layer [270] can be formed adjacent to the amorphous silicon I-layer [260]. The amorphous silicon P-layer [270] forms an outer layer of each of the image sensors. The amorphous silicon P-layer [270] can include P-layer ion implantation regions [420] that provide physical isolation between the outer layers of the image sensors.

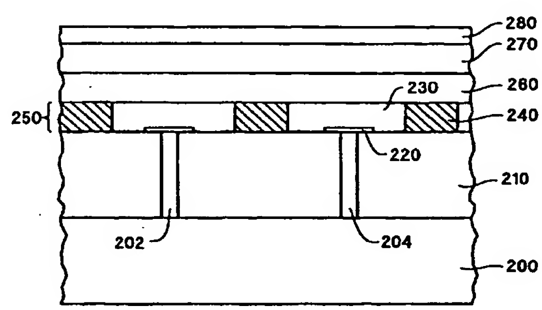

Figure 2

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Description

[0001] This invention relates generally to an image sensor array device, such as PIN photo diode image sensors. In particular, it relates to a plurality of elevated PIN diode image sensors in which the diode image sensor are physically isolated from each other by ion implantation regions.

[0002] An array of image sensors or light sensitive sensors detect the intensity of light received by the image sensors. The image sensors typically generate electronic signals that have amplitudes that are proportionate to the intensity of the light received by the image sensors. The image sensors can convert an optical image into a set of electronic signals. The electronic signals may represent intensities of colors of light received by the image sensors. The electronic signals can be conditioned and sampled to allow image processing.

[0003] Integration of the image sensors with signal processing circuitry is becoming more important because integration enables miniaturization and simplification of imaging systems. Integration of image sensors along with analog and digital signal processing circuitry allows electronic imaging systems to be low cost, compact and require low power consumption.

[0004] Historically, image sensors have predominantly been charged coupled devices (CCDs). CCDs are relatively small and can provide a high-fill factor. However, CCDs are very difficult to integrate with digital and analog circuitry. Further, CCDs dissipate large amounts of power and suffer from image smearing problems.

[0005] An alternative to CCD sensors are active pixel sensors. Active pixel sensors can be fabricated using standard CMOS processes. Therefore, active pixel sensors can easily be integrated with digital and analog signal processing circuitry. Further, CMOS circuits dissipate small amounts of power.

[0006] Figure 1 shows a cross-section of a prior art array of image sensors. This array of image sensors includes PIN diode sensors located over a substrate 10. An interconnection structure 12 electrically connects an N-layer 14 of the PIN diodes to the substrate 10. An I-layer 16 is formed over the N-layer 14. A P-layer 18 is formed over the I-layer 16. The P-layer 18, the I-layer 16 and the N-layer 14 form the array of PIN diode sensors. A first conductive via 20 electrically connects a first diode sensor to the substrate 10, and a second conductive via 22 electrically connects a second diode sensor to the substrate 10. A transparent conductive layer 24 is located over the array of diode sensors. A conductive lead 26 is connected to the transparent conductive layer 24. The conductive lead 26 is connected to a bias voltage which allows biasing of the P-layer 18 of the array of PIN diode sensors to a selected voltage potential.

[0007] A limitation of the image sensor structure of Figure 1 is that the individual image sensors are not isolated from each other. That is, light received by a given image sensor effects neighboring image sensors because current can flow through the N-layer 14 between neighboring image sensors. Charge flows between the image sensors particularly when the light intensity of the received light varies greatly between neighboring image sensors. The P-layer 18, the I-layer 16 and the N-layer 14 are shared by neighboring image sensors. A trench 28 is formed to provide some isolation between the image sensors by increasing the resistance between the N-layers sections of neighboring image sensors.

[0008] It is desirable to have a plurality of active pixel sensors formed adjacent to a substrate in which the pixel sensors are isolated from each other to reduce coupling between the pixel sensors. It is desirable that the process required to form the isolated pixel sensor be easy to implement.

[0009] The invention includes an array of image sensors formed adjacent to a substrate. The array includes ion implantation regions located between the image sensors. The ion implantation regions provide physical isolation between image sensors. The physical isolation reduces coupling and cross-talk between the image sensors. The array of isolated image sensors can be formed by a simple fabrication process.

[0010] A first embodiment includes an image sensor array. The image sensor array includes a substrate. An interconnect structure is formed adjacent to the substrate. An amorphous silicon electrode layer is adjacent to the interconnect structure. The amorphous silicon electrode layer includes electrode ion implantation regions between pixel electrode regions. The pixel electrode regions define cathodes of an array of image sensors. The electrode ion implantation regions provide physical isolation between the pixel electrode regions. The cathodes are electrically connected to the interconnect structure. An amorphous silicon I-layer is adjacent to the amorphous silicon electrode layer. The amorphous silicon I-layer forms an inner layer of each of the image sensors. A transparent electrode layer is formed adjacent to the image sensors. An inner surface of the transparent electrode is electrically connected to anodes of the image sensors and the interconnect structure.

[0011] A second embodiment is similar to the first embodiment. The amorphous silicon I-layer region of the second embodiment includes I-layer ion implantation regions that provide physical isolation between the inner layers of the image sensors. The I-layer ion implantation regions align with the electrode ion implantation regions.

[0012] A third embodiment is similar to the first embodiment. The third embodiment includes an amorphous silicon P-layer adjacent to the amorphous silicon I-layer. The amorphous silicon P-layer forms an outer layer of each of the image sensors.

[0013] A fourth embodiment is similar to the third embodiment. The amorphous silicon P-layer region of

the fourth embodiment includes P-layer ion implantation regions that provide physical isolation between the outer layers of the image sensors.

[0014] Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

Figure 1 shows a cross-section of a prior art array of image sensors.

Figure 2 shows an embodiment of the invention.

Figure 3 shows another embodiment of the invention.

Figure 4 shows another embodiment of the invention.

Figure 5 shows another embodiment of the invention.

Figures 6-11 show processing steps which can be used to fabricate the embodiments of the invention shown in Figure 2 and Figure 5.

Figure 12 is a flow chart showing the steps of a method of forming the embodiments of the invention.

[0015] As shown in the drawings for purposes of illustration, the invention is embodied in an elevated image sensor array adjacent to a substrate which includes isolation between the image sensors. The ion implantation regions provide physical isolation between image sensors. The physical isolation reduces coupling and cross-talk between the image sensors. The array of isolated image sensors can be formed by a simple fabrication process.

[0016] Figure 2 shows a first embodiment of the invention. This embodiment includes a substrate 200. An interconnection structure 210 is formed adjacent to the substrate 200. Inner metal sections 220 are formed adjacent to the interconnect structure 210. An electrode layer 250 is formed adjacent to the interconnect structure 210. The electrode layer 250 covers the inner metal sections 220. The electrode layer 250 includes electrode ion implantation regions 240 and pixel electrodes 230. The locations of the electrode ion implantation regions 240 define the locations of the pixel electrodes 230. The electrode ion implantation regions 240 provide physical isolation between the pixel electrodes 230. The pixel electrodes 230 form cathodes of an array of image sensors.

[0017] This embodiment further includes an inner layer 260 adjacent to the electrode layer 250, and an outer layer 270 adjacent to the inner layer 260. A transparent conductor 280 is adjacent to the outer layer 270. Each image sensor of the array of image sensors includes an individual inner metal section 220 and a pixel electrode 230.

[0018] The pixel electrode 230 of a first image sensor is electrically connected to the substrate 200 through a first conductive via 202. The pixel electrode 230 of a second image sensor is electrically connected to the substrate 200 through a second conductive via 204.

[0019] The image sensors conduct charge when the image sensors receive light. The substrate 200 generally includes sense circuitry and signal processing circuitry. The sense circuitry senses how much charge the image sensors have conducted. The amount of charge conducted represents the intensity of light received by the image sensors. Generally, the substrate 200 can be CMOS (complementary metal oxide silicon), BiCMOS or Bipolar. The substrate 200 can include various types of substrate technology including charged coupled devices.

[0020] Typically, the interconnection structure 210 is a standard CMOS interconnection structure. The structure and methods of forming this interconnection structure 210 are well known in the field of electronic integrated circuit fabrication. The interconnection structure 210 can be a subtractive metal structure, or a single or dual damascene structure.

[0021] The conductive vias 202, 204 pass through the interconnect structure 210 and electrically connect the pixel electrodes 230 to the substrate 200. Typically, the conductive vias 202, 204 are formed from tungsten. Tungsten is generally used during fabrication because tungsten can fill high aspect ratio holes. That is, tungsten can be used to form narrow and relatively long interconnections. Typically, the conductive vias 202, 204 are formed using a chemical vapor deposition (CVD) process. Other materials which can be used to form the conductive vias 202, 204 include copper, aluminum or any other electrically conductive material.

[0022] There are several structural advantages to having the pixel interconnect structure 210 between the pixel electrodes 230 and the substrate 200. This structure allows the interconnection circuitry to be tightly packed. First of all, lateral space is conserved because the vias 202, 204 are located directly underneath the pixel electrodes. Secondly, the structure allows the formation of vias 202, 204 having a minimal diameter. CVD processes are generally the best method of forming the vias 202, 204. A Tungsten CVD process allows for the formation of small diameter vias. However, the temperatures required to form tungsten vias with a CVD process are greater than many of the materials (amorphous silicon for example) to form the pixel electrodes can withstand. By forming the pixel interconnect structure 210 over the substrate 200, and the pixel electrodes 220 over the pixel interconnect structure 210, the vias 202, 204 can be formed before the pixel electrodes 220, and

therefore, the pixel electrodes 230 are not subjected to the high temperatures required for the formation of the vias 202, 204.

[0023] The inner metal sections 220 should include a thin conductive material. The inner metal sections 220 may be formed, for example, from a degenerately doped semiconductor layer, aluminum, titanium, titanium nitride, copper or tungsten. The inner metal sections 220 should be thin (approximately 500 Angstroms) and smooth. The inner metal sections 220 should be smooth enough that any surface roughness is substantially less than the thickness of the pixel electrodes 230 formed over the inner metal sections 220. To satisfy the smoothness requirement, polishing of the inner metal sections 220 may be required.

[0024] The inner metal sections 220 can be optional. However, the inner metal sections 220 have a lower resistance than the materials used to form the pixel electrodes 230. Therefore, the inner metal sections 220 provide better current collection.

[0025] The amorphous silicon electrode layer 250 includes both the pixel electrodes 230 and the electrode ion implantation regions 240. The electrode layer 250 is generally formed from a doped semiconductor. The doped semiconductor can be an N-layer of amorphous silicon.

[0026] The electrode layer is typically deposited using plasma etched chemical vapor deposition (PECVD). A silicon containing gas (such as Si_2H_6 or SiH_4) is included when forming an amorphous silicon electrode layer 250. When forming an N-layer electrode layer 250, the PECVD process is performed with a phosphorous containing gas (such as PH_3).

[0027] The electrode ion implantation regions 240 are formed according to a predetermined pattern. The electrode ion implantation regions 240 define the pixel electrodes 230, and provide physical isolation between the pixel electrodes 230. Ion implantation regions have been used for providing electrical isolation between active devices, but not for the purpose of providing physical isolation between image sensors of an array of image sensors. Elements which can be implanted to provide the electrode ion implantation regions 240 include N, Ar, O, B, F and C. Etched Si or Ge can also serve as electrode ion implantation regions 240. Isolation is provided by further amorphizing an alpha silicon layer (the electrode layer) between the image sensors (pixels). The etched Si or Ge, or ion implantation regions 240 disrupt the short range order of the amorphous silicon to prevent conduction of holes and electrons in the disrupted areas.

[0028] The ion implantation regions 240 are typically formed by coating a resist on the amorphous silicon electrode layer 250, and removing the resist according to a predetermined pattern where the ion implantation regions 240 are to be formed. Methods of coating and selectively removing resist are well known in the art of semiconductor processing. Ions are then implanted in the exposed regions of the amorphous silicon electrode layer 250. Methods of implanting ions are also well known in the art of semiconductor processing.

[0029] The pixel electrodes 230 must be thick enough, and doped heavily enough that the pixel electrodes 230 do not fully deplete when biased during operation. The pixel electrodes 230 are typically doped with phosphorous.

[0030] An N-layer of amorphous silicon is typically used electrode layer 250 when forming PIN diode image sensors. However, the diode image sensors can include an NIP sensor configuration. In this case, the electrode layer 250 is formed from a P-layer.

[0031] The inner layer 260 is typically an I-layer which is formed from hydrogenated amorphous silicon. The I-layer can be deposited using a PECVD process or a reactive sputtering process. The PECVD process must include a silicon containing gas. The deposition should be at a low enough temperature that hydrogen is retained within the film. The I-layer is typically on the order of one micron thick.

[0032] The outer layer 270 is typically a P-layer 270 which is formed from amorphous silicon. Typically, the P-layer is doped with Boron.

[0033] The P-layer can deposited using a PECVD process. The PECVD process is performed with a Boron containing gas. The Boron containing gas can be B_2H_6. A silicon containing gas is included when forming an amorphous silicon P-layer. The thickness of the P-layer must generally be controlled to ensure that the P-layer does not absorb too much short wavelength (blue) light.

[0034] Another embodiment of the invention does not include the P-layer outer layer 270. The P-layer can be eliminated with proper selection of the composition of the material within the transparent conductor 280, and proper selection of the doping levels of the pixel electrodes 230. For this embodiment, the transparent conductor 280 provides an electrical connection between a top surface of the I-layer inner section 260 of the image sensors and the interconnection structure 210.

[0035] As previously described, the pixel electrodes 230, the inner layer 260 and the outer layer 270 are generally formed from amorphous silicon. However, the pixel electrodes 230, the inner layer 260 and the outer layer 270 can also be formed from amorphous carbon, amorphous silicon carbide, amorphous germanium, or amorphous silicon-germanium. It should be understood that this list is not exhaustive.

[0036] The transparent conductor 280 provides a conductive connection between anodes of the image sensors (typically the outer layer 270) and the interconnection structure 210. Light must pass through the transparent conductor 280 which is received by the image sensors. Generally, the transparent conductor 280 is formed from an indium tin oxide. However, the transparent conductor 280 can also be formed from tita-

nium nitride, thin silicide, or certain types of transition metal nitrides or oxides.

[0037] Both the selection of the type of material to be used within the transparent conductor 280, and the determination of the desired thickness of the transparent conductor 280, are based upon minimizing the optical reflection of light received by the image sensor. Minimization of the reflection of light received by the image sensor helps to optimize the amount of light detected by the image sensor.

[0038] The transparent conductor 280 can be deposited by a sputtering process. Deposition through sputtering is well known in the art of integrated circuit fabrication.

[0039] A protective layer may be formed over the transparent conductor 280. The protective layer provides mechanical protection, electrical insulation, and can provide some anti-reflective characteristics.

[0040] Figure 3 shows another embodiment of the invention. For this embodiment, rather than several image sensors sharing an inner layer 260 I-layer, each image sensor includes an individual I-layer section 310. That is, each PIN diode sensor image sensors includes a separate I-layer section 310.

[0041] Similar to the pixel electrodes 230, the I-layer sections 310 are formed between I-layer ion implantation regions 320. The I-layer ion implantation regions 320 are generally formed according to the same predetermined pattern as the electrode ion implantation regions 240. The I-layer ion implantation regions 320 define the I-layer sections 310, and provide physical isolation between the I-layer sections 310. Ion implantation regions have been used for providing electrical isolation between active devices, but not for the purpose of providing physical isolation between image sensors of an array of image sensors. Elements which can be implanted to provide the I-layer ion implantation regions 320 include N, Ar, O, B, F and C. Etched Si or Ge can also serve as I-layer ion implantation regions 320. Isolation is provided by further amorphizing an alpha silicon layer (the inner layer 260) between the image sensors (pixels). The etched Si or Ge, or ion implantation regions 240 disrupt the short range order of the amorphous silicon to prevent conduction of holes and electrons in the disrupted areas.

[0042] The method of forming the I-layer ion implantation regions 320 can be the same as the method of forming the ion implantation regions 240 as described above.

[0043] Figure 4 shows another embodiment of the invention. For this embodiment, rather than several image sensors sharing an outer layer 270 P-layer, each image sensor includes an individual P-layer section 410. That is, each PIN diode sensor image sensor includes a separate P-layer section 410.

[0044] Similar to the pixel electrodes 230, the P-layer sections 410 are formed between P-layer ion implantation regions 420. The P-layer ion implantation regions 420 are generally formed according to the same predetermined pattern as the electrode ion implantation regions 240. The P-layer ion implantation regions 420 define the P-layer sections 410, and provide physical isolation between the P-layer sections 410. Ion implantation regions have been used for providing electrical isolation between active devices, but not for the purpose of providing physical isolation between image sensors of an array of image sensors. Elements which can be implanted to provide the P-layer ion implantation regions 420 include N, Ar, O, B, F and C. Etched Si or Ge can also serve as P-layer ion implantation regions 420. Isolation is provided by further amorphizing an alpha silicon layer (the outer layer 270) between the image sensors (pixels). The etched Si or Ge, or ion implantation regions 240 disrupt the short range order of the amorphous silicon to prevent conduction of holes and electrons in the disrupted areas.

[0045] The method of forming the P-layer ion implantation regions 420 can be the same as the method of forming the ion implantation regions 240 as described above.

[0046] Figure 5 shows another embodiment of the invention. This embodiment includes an inner surface of the transparent conductor 280 being electrically connected to the substrate 200 through a third conductive via 502. The embodiment shown in Figure 5 only includes the pixel electrodes 230 and electrode ion implantation regions 240 of the electrode layer 250. However, the I-layer sections 310 and I-layer ion implantation regions 320 of the inner layer 260 I-layer of Figure 3 can be included. Additionally, the P-layer sections 410 and P-layer ion implantation regions 420 of the outer layer 270 P-layer of Figure 4 can also be included.

[0047] Figures 6-11 show processing steps which can be used to fabricate the embodiments of the invention shown in Figure 2 and Figure 5.

[0048] Figure 6 shows a substrate 200 with a standard interconnect structure 210 formed over the substrate 200. Inner metal layer sections 220, an electrode layer 250 and a photo-resist layer 610 are deposited over the interconnect structure 210.

[0049] The structure and methods of forming this interconnect structure 210 are well known in the field of electronic integrated circuit fabrication. The interconnect structure 210 can be a subtractive metal structure, or a single or dual damascene structure.

[0050] The pixel interconnect structure 210 includes conductive vias 202, 204, 502. Generally, the conductive vias 202, 204, 502 are formed from tungsten. Tungsten is generally used because during fabrication, tungsten can fill high aspect ratio holes. That is, tungsten can be used to form narrow and relatively long interconnections. Typically, the conductive vias 202, 204, 502 are formed using a chemical vapor deposition (CVD) process. Other materials which can be used to form the conductive vias 202, 204, 502 include copper, aluminum or any other electrically conductive material.

[0051] The inner metal layer 60 is typically deposited by a sputtering process.

[0052] As previously stated, the electrode layer 250 is typically deposited using plasma etched chemical vapor deposition (PECVD). A silicon containing gas (such as Si_2H_6 or SiH_4) is included when forming an amorphous silicon electrode layer 250. When forming an N-layer electrode layer 250, the PECVD process is performed with a phosphorous containing gas (such as PH_3).

[0053] The photo-resist layer 610 is deposited over the interconnect structure 210. Deposition of photoresist 610 is a process which is well understood in the art of semiconductor processing.

[0054] Figure 7 shows the photo-resist 610 in which a predetermined pattern of the photo-resist have been removed. The islands of photo-resist which are not removed, define the locations of the pixel electrodes 230 of the electrode layer 250. the portions of photoresist which have been removed define the locations of the electrode implantation regions 240. Methods of removing photo-resist are well known in the art of semiconductor processing.

[0055] The arrows 710 of Figure 7 show where the ions of the select group of materials are implanted. As previously mentioned, the materials which can be implanted include N, Ar, O, B, F and C. Etched Si or Ge can also serve as electrode ion implantation regions 240.

[0056] Figure 8 shows the patterned photo-resist layer having been removed. Figure 8 also shows the pixel electrodes 230 and the electrode ion implantation regions 240.

[0057] Figure 9 shows the inner layer 260 and the outer layer 270 having been deposited over the electrode layer 250. As previously stated, the inner layer 260 is typically an I-layer, and the outer layer 270 is typically a P-layer. The structure shown in Figure 9 is similar to the embodiment of Figure 2. Deposition of a transparent conductor 280 over the structure shown in Figure 9 results in the embodiment shown in Figure 2.

[0058] The I-layer is generally deposited using a PECVD process or reactive sputtering process. The PECVD process must include a silicon containing gas. The deposition should be at a low enough temperature that hydrogen is retained within the film.

[0059] The P-layer can also be deposited using a PECVD process. The PECVD process is performed with a Boron containing gas. The Boron containing gas can be B_2H_6. A silicon containing gas is included when forming an amorphous silicon P-layer.

[0060] Figure 10 shows the the electrode layer 250, the inner layer 260 and the outer layer 270 having been wet or dry etched according to a predetermined pattern to allow access to the third conductive via 502.

[0061] Figure 11 shows the transparent conductive layer 280 deposited over the outer layer 270. The transparent conductive layer 280 provides an electrical connection between the outer layer 270 and the conductive via 56. Generally, the transparent conductor 280 is formed from an indium tin oxide. However, the transparent conductor 280 can also be formed from titanium nitride, thin suicide, or certain types of transition metal nitrides or oxides.

[0062] The transparent conductive layer 280 is generally deposited through reactive sputtering. However, the transparent conductive layer 280 can also be grown by evaporation. If the transparent conductive layer 280 is formed from titanium nitride, then typically a CVD process or a sputtering process must be used to deposit the transparent conductive layer 280.

[0063] As stated previously, a protective layer may be formed over the transparent conductor 280. The protective layer provides mechanical protection, electrical insulation, and can provide some anti-reflective characteristics.

[0064] Figure 12 is a flow chart showing the steps of a method of forming the embodiments of the invention. A first step 1210 includes forming an interconnect structure over a substrate. A second step 1220 includes depositing a pixel electrode layer over the interconnect structure. A third step 1230 includes depositing a photoresist over the electrode layer. A fourth step 1240 includes patterning the photo-resist layer according to a predetermined pattern. A fifth step 1250 includes implanting ions in the electrode layer where the photoresist has been removed. A sixth step 1260 includes removing the patterned photo-resist layer. A seventh step 1270 includes depositing a I-layer over the pixel electrode layer. An eighth step 1280 includes depositing a P-layer over the I-layer. Finally, a ninth step 1290 includes depositing a transparent conductor layer electrically connecting the outer surface of the image sensors to the interconnect structure.

[0065] The third step 1230, the fourth step 1240, and the fifth step 1250 can be repeated for both the I-layer and the P-layer to form the I-layer implantation regions and the P-layer implantation regions.

[0066] Although specific embodiments of the invention have been described and illustrated, the invention is not to be limited to the specific forms or arrangements of parts so described and illustrated. The invention is limited only by the claims.

Claims

1. An image sensor array device comprising:

   a substrate [200];
   an interconnect structure [210] adjacent to the substrate [200];
   an amorphous silicon electrode layer [250] adjacent to the interconnect structure [210], the amorphous silicon electrode layer [250] comprising electrode ion implantation regions [240] between pixel electrode regions [230], the pixel

electrode regions [230] defining cathodes of an array of image sensors, the electrode ion implantation regions [240] providing physical isolation between the pixel electrode regions [230], the cathodes electrically connected to the interconnect structure [210];

an amorphous silicon I-layer [260] adjacent to the amorphous silicon electrode layer [250], the amorphous silicon I-layer [260] forming an inner layer of each of the image sensors; and a transparent electrode layer [280] formed adjacent to the image sensors, an inner surface of the transparent electrode layer [280] electrically connected to anodes of the image sensors and the interconnect structure [210].

2. The image sensor array as recited in claim 1, wherein the amorphous silicon I-layer [260] comprises I-layer ion implantation regions [320] that provide physical isolation between the inner layers of the image sensors, the I-layer ion implantation regions [320] aligning with the electrode ion implantation regions [240].

3. The image sensor array as recited in claim 1, further comprising an amorphous silicon P-layer [270] adjacent to the amorphous silicon I-layer [260], the amorphous silicon P-layer [270] forming an outer layer of each of the image sensors.

4. The image sensor array as recited in claim 3, wherein the amorphous silicon P-layer [270] comprises P-layer ion implantation regions [420] that provide physical isolation between the outer layers of the image sensors.

5. The image sensor array as recited in claim 1, wherein the amorphous silicon electrode layer [250] comprises an N-layer.

6. The image sensor array as recited in claim 1, wherein the interconnect structure [210] electrically interconnects the pixel electrode regions [230] to the substrate [200].

7. The image sensor array as recited in claim 1, wherein the inner surface of the transparent electrode layer [280] is electrically connected to the interconnect structure 210] through a tungsten plug [502].

8. The image sensor array as recited in claim 1, wherein the transparent electrode layer [280] comprises indium tin oxide.

9. The image sensor array as recited in claim 1, wherein implantation regions [240] comprise Boron implants, Nitrogen implants, Argon implants, or Oxide implants.

10. The image sensor array as recited in claim 1, wherein the substrate comprises CMOS.

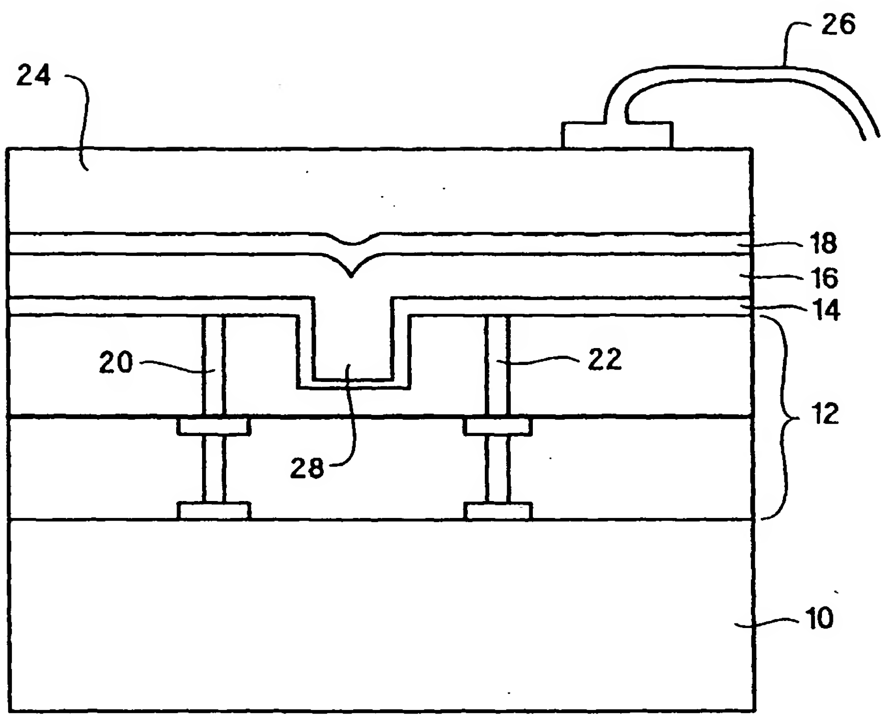

Figure 1 (Prior Art)

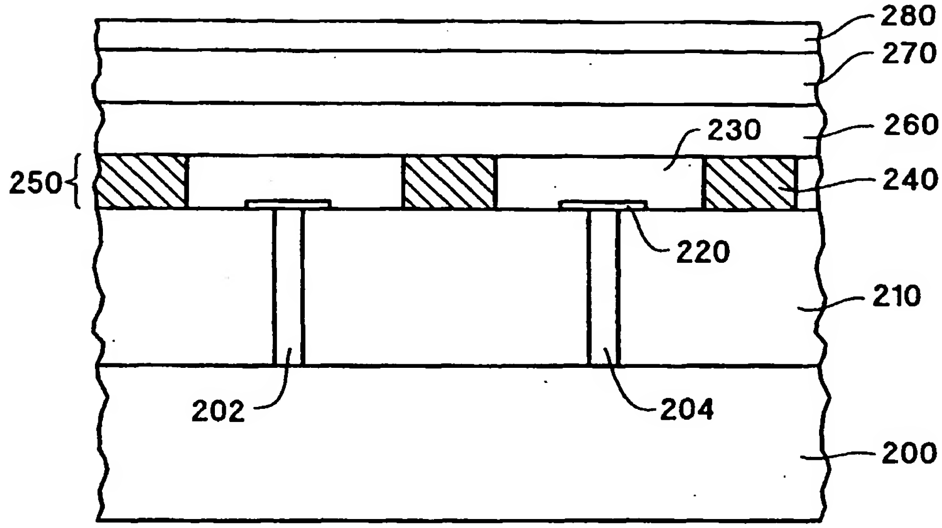

Figure 2

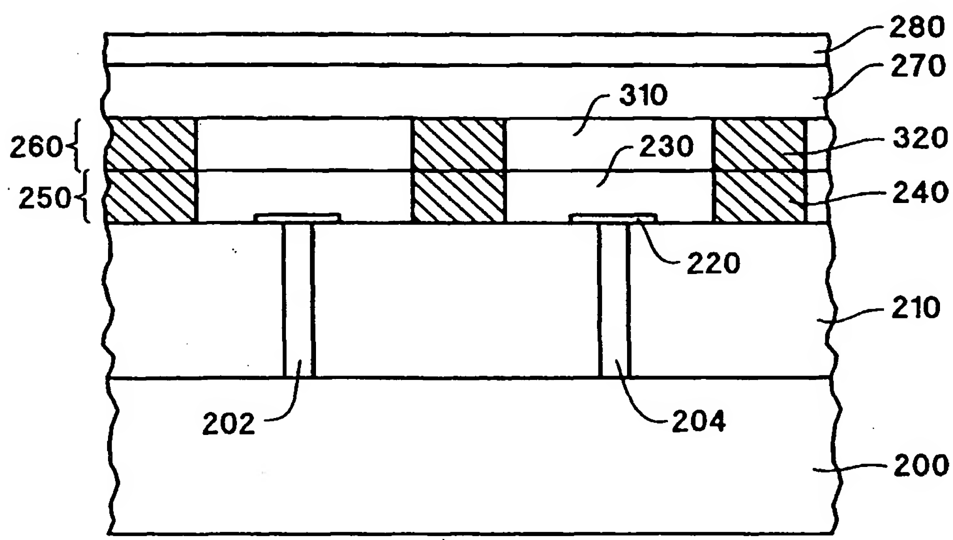

Figure 3

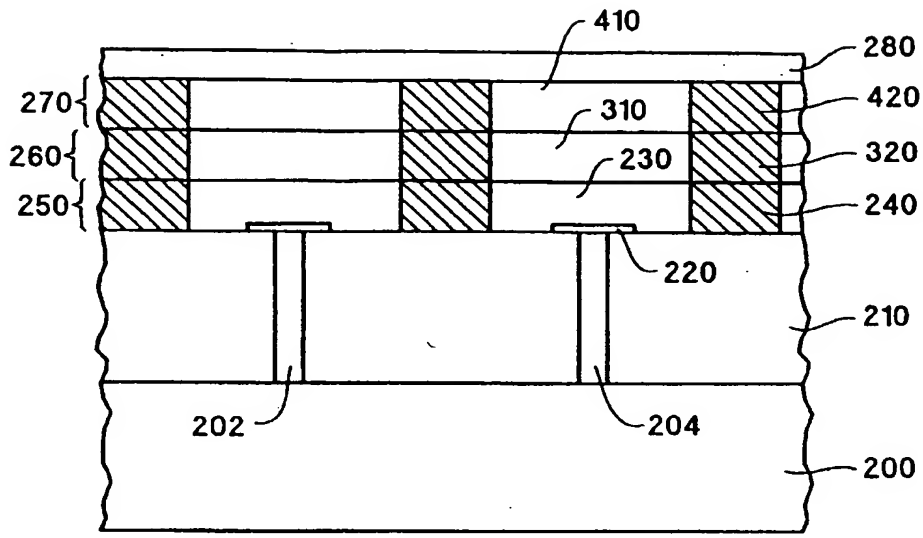

Figure 4

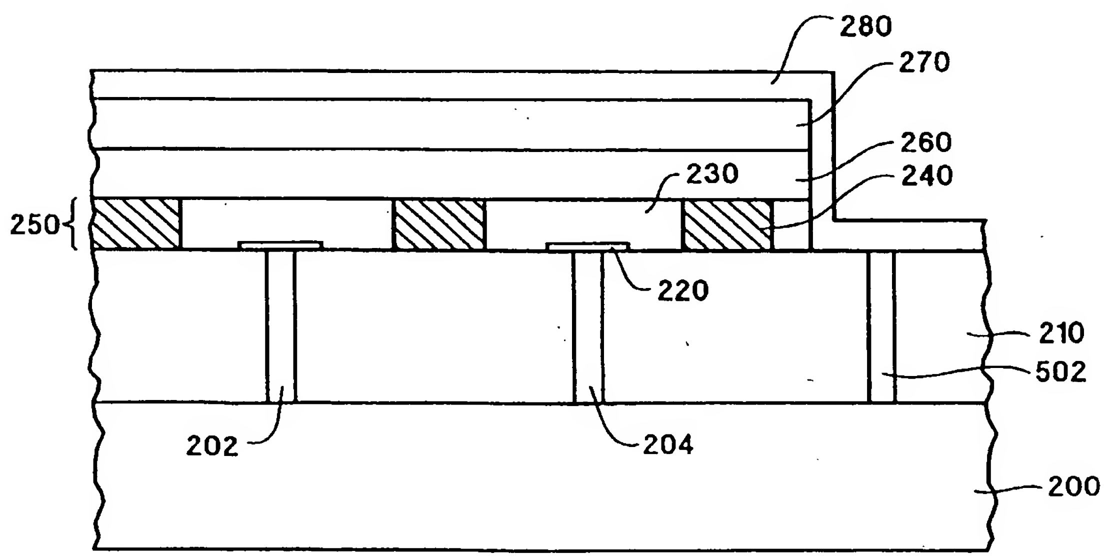

Figure 5

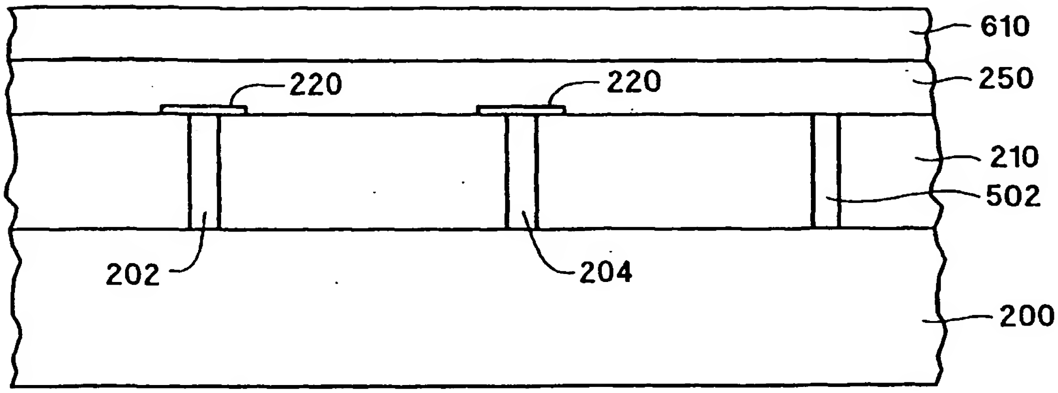

Figure 6

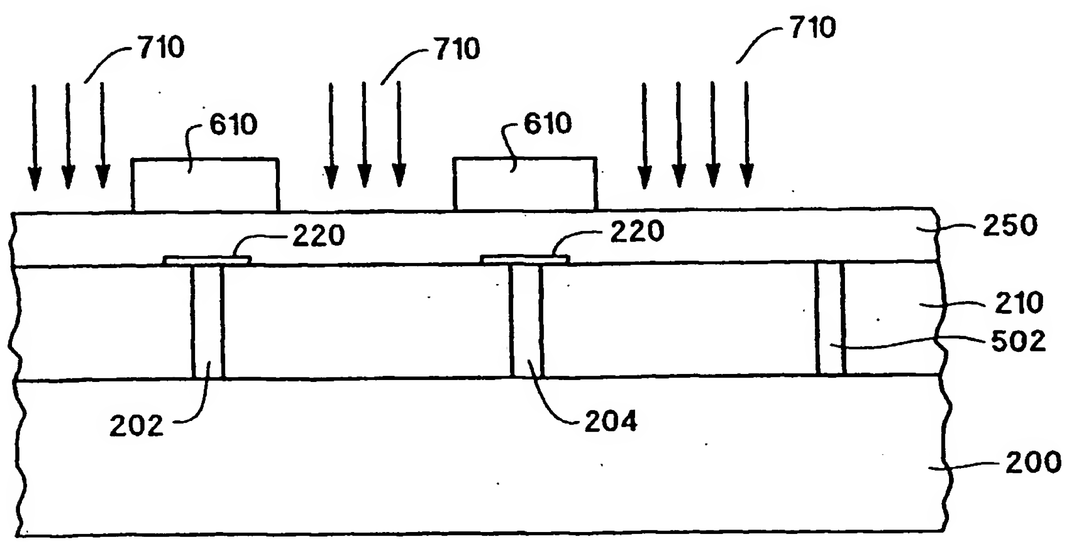

Figure 7

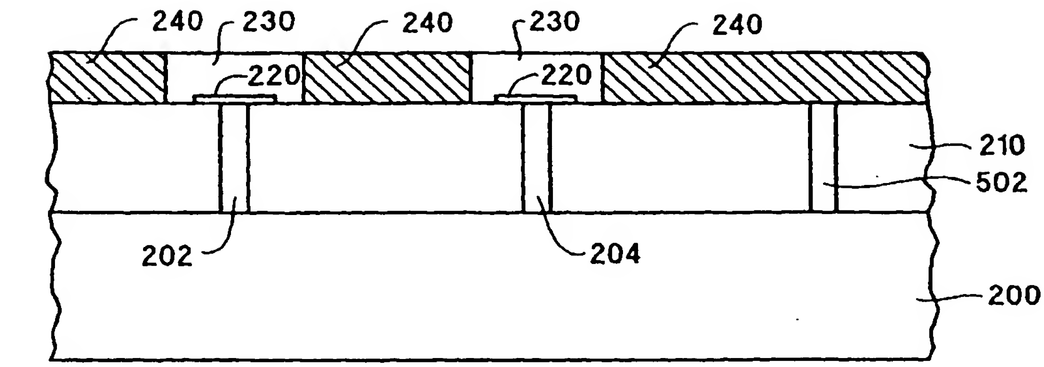

Figure 8

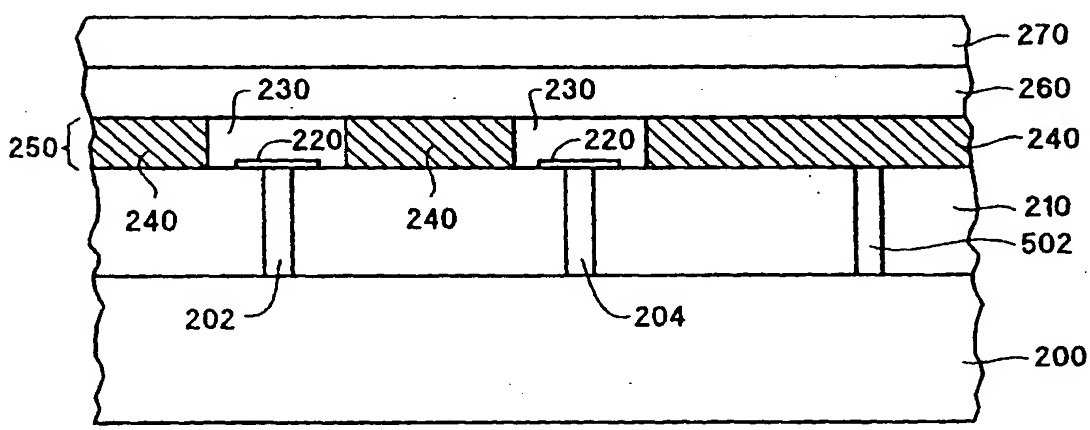

Figure 9

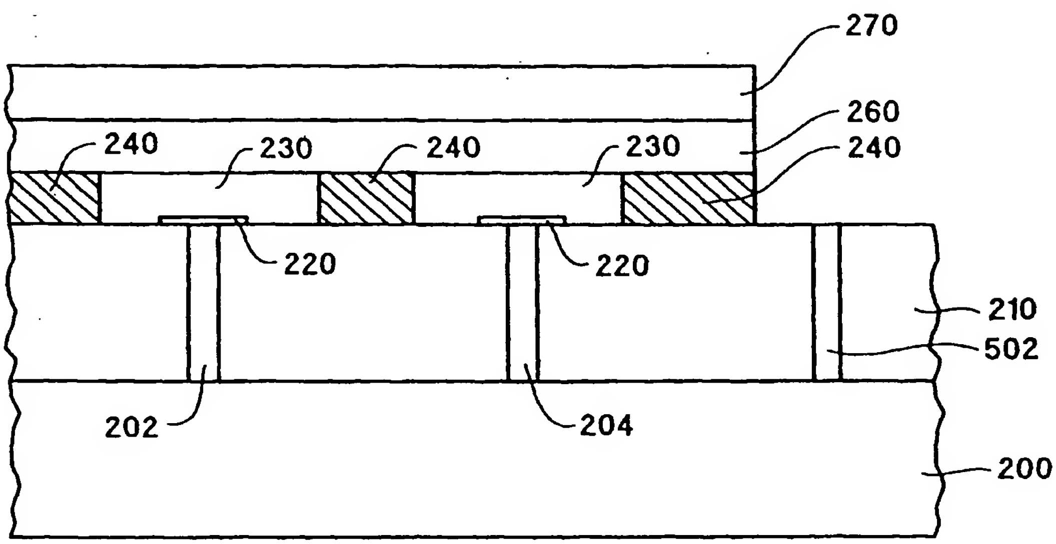

Figure 10

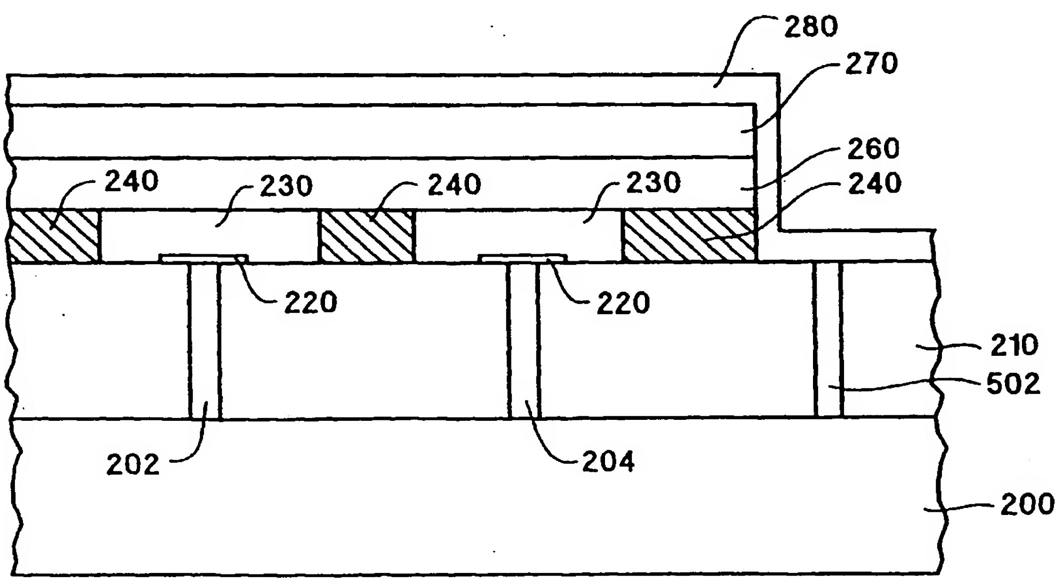

Figure 11

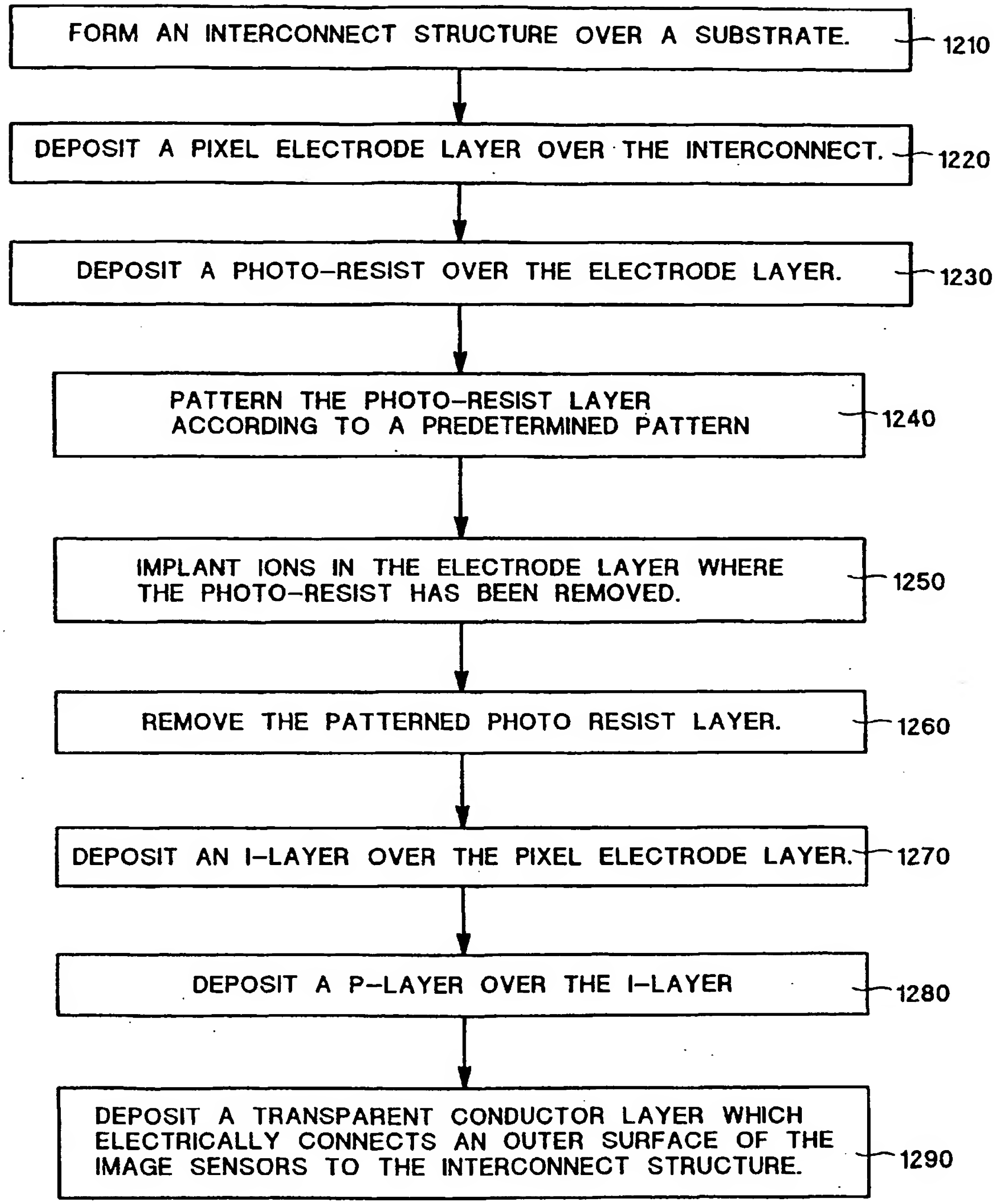
FORM AN INTERCONNECT STRUCTURE OVER A SUBSTRATE.
1210
DEPOSIT A PIXEL ELECTRODE LAYER OVER THE INTERCONNECT.
1220
DEPOSIT A PHOTO-RESIST OVER THE ELECTRODE LAYER.
1230
PATTERN THE PHOTO-RESIST LAYER ACCORDING TO A PREDETERMINED PATTERN
1240
IMPLANT IONS IN THE ELECTRODE LAYER WHERE THE PHOTO-RESIST HAS BEEN REMOVED.
1250
REMOVE THE PATTERNED PHOTO RESIST LAYER.
1260
DEPOSIT AN I-LAYER OVER THE PIXEL ELECTRODE LAYER.
1270
DEPOSIT A P-LAYER OVER THE I-LAYER
1280
DEPOSIT A TRANSPARENT CONDUCTOR LAYER WHICH ELECTRICALLY CONNECTS AN OUTER SURFACE OF THE IMAGE SENSORS TO THE INTERCONNECT STRUCTURE.
1290

Figure 12